Application No.: 09/771,547 Docket No.: D-1059

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of:
Toshiyuki SATO et al.

Application No.: 09/771,547 Group Art Unit: 2615

Filed: January 30, 2001 Examiner: Y.K. Aggarwal

For: RADIATION DETECTOR

APPEAL BRIEF UNDER 37 CFR § 41.37

Date: September 18, 2006

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action of May 18, 2006, reinstatement of the appeal is requested.

This Appeal Brief is filed pursuant to 37 CFR § 41.37 in response to the Office Action dated May 18, 2006 rejecting all pending claims after prosecution was reopened.

On month extension of time is hereby requested. A credit card authorization form in the amount of $120.00 is attached herewith for the one month extension of time. If any other fee is required, please charge to Deposit Account No. 11-0219.

REAL PARTY IN INTEREST

The real party in interest is Assignee Shimadzu Corporation.

RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' representative, and the Assignee of this application are aware of no other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on, the Board's decision in the pending appeal.

STATUS OF CLAIMS

This is an appeal from the non-final rejection of claims 1, 4, 5, and 7 as presented in the Office Action of May 18, 2006.

Claims 1, 4, 5, and 7 are pending in the application. Each of claims 1, 4, 5, and 7 stands rejected, and the rejection of each of claims 1, 4, 5, and 7 is appealed.

Claims 1, 4, 5, and 7 on appeal are set forth in their entirety in the Claims Appendix attached hereto.

STATUS OF AMENDMENTS

Each of the claim amendments presented in Appellants' Amendment filed November 23, 2005 has been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a radiation detector for industrial and medical purposes, and more particularly, to a direct-converting-type radiation detector using a converting layer for absorbing light or radiation to generate a pair of electron-holes.

As disclosed in Appellants' specification (page 4, line 4, through page 5, line 5), in a conventional two-dimensional

radiation image detector wherein the amorphous selenium (a-Se) as the converting layer is directly formed on the active matrix board by a vapor deposition method, there are the following problems:

(1) In case semiconductor materials other than amorphous selenium (a-Se) as the converting layer 1 are used, semiconductor materials to be used are restricted due to a heat resistance problem of the active matrix board 10. For example, in case a polycrystalline film of CdTe or CdZnTe having a more improved sensitivity with respect to X-rays when compared with amorphous selenium is formed by a MOCVD method, proximity sublimation method, paste baking method or the like, which is suitable for forming a large area film, a film forming temperature higher than 300°C is required. However, generally, a heat resistant temperature of the switching element (TFT) 3 formed on the active matrix board 10 is about 250°C, in case the amorphous silicone (a-Si:H) is used as a normal semiconductor layer. Therefore, there is a difficulty in directly forming a polycrystalline film of CdTe and CdZnTe on the active matrix board 10 of a-Si:H.

(2) In a large two-dimensional picture image detector, wirings of the gate lines 4 and data lines 5 in the active matrix board 10 become long, and the gate lines 4 and the data lines 5 are connected to the gate driving circuit 6 and signal reading-out circuit 7 through flexible panel circuits (FPC) by using anisotropic conductive films (ACF) and the like. In this case, there is a problem such that noises are generated by these parasitic resistance and capacitance component to thereby deteriorate a signal to noise (S/N) ratio and a dynamic range as important performances of the two-dimensional picture image detector.

In view of the above-described problems, the present invention was developed. An object of the invention is to provide "a radiation detector, wherein a high thermal resistant matrix process board is used so that polycrystalline films of CdTe, CdZnTe and the like can be directly formed thereon, to thereby provide a low signal to noise (S/N) ratio and prevent reduction of a dynamic range caused by connection of circuits" (specification page 5, lines 6-12).

Therefore, the invention as defined in claim 1 is directed to a radiation detector including an active matrix board including gate lines and data lines arranged in a two-dimensional lattice shape, a plurality of high-speed switching elements provided at respective lattice points and connected to the gate lines and the data lines, each switching element being formed of a polycrystalline silicon thin film transistor and having a source electrode, pixel electrodes connected to the source electrodes of the high-speed switching elements, and charge storage capacitances, each being disposed between the pixel electrode and a ground electrode (specification page 7, lines 9-25).

The detector includes a converting layer, formed on the pixel electrodes, to generate a pair of electron-holes by absorbing radiation (specification page 7, lines 25-27). The converting layer is formed of a vapor-deposited polycrystalline film of CdTe or CdZnTe (specification page 10, line 22).

Therefore, with the present invention, a two-dimensional picture image detector can be structured by using a polycrystalline semiconductor film, such as CdTe and CdZnTe, having a high sensitivity with respect to radiation, as a converting layer.

The invention as defined in independent claim 7 is directed to a radiation detector including an active matrix board including gate lines and data lines arranged in a two-dimensional lattice shape, a plurality of high-speed switching elements provided at respective lattice points and connected to the gate lines and the data lines, each switching element being formed of a polycrystalline silicon thin film transistor with a heat resistant temperature of more than 300°C and having a source electrode, pixel electrodes connected to the source electrodes of the high-speed switching elements, and charge storage capacitances, each being disposed between the pixel electrode and a ground electrode (specification page 7, lines 9-25; the "heat resistant temperature of more than 300°C" is disclosed at page 8, lines 17-24).

The detector includes a converting layer, formed on the pixel electrodes, to generate a pair of electron-holes by absorbing radiation (specification page 7, lines 25-27). The converting layer is a vapor-deposited polycrystalline film of CdTe or CdZnTe having a film-forming temperature higher than 300°C (specification page 10, lines 22-24).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

35 U.S.C. § 103(a) - Appellants' "admitted prior art" in view of Ikeda et al.

Claims 1, 4, and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Appellants' "admitted prior art" in view of U.S. Patent No. 6,403,965 to Ikeda et al. (hereinafter "Ikeda").

The Office Action acknowledges that "Applicant's admitted prior art does not explicitly teach that each high-speed switching elements are formed of polycrystalline silicon thin film transistors."

The Office Action relies upon Ikeda for its teaching of "an X-ray image detector system wherein the TFTs may be formed of polysilicon (figures 1 and 2 show the TFT 701) in order to decrease the size of a TFT so that the effective area of each pixel can be increased (col.12 lines 1-10).

The Office Action concludes that "it would have been obvious . . . to have been motivated to have used poly-silicon as the material for TFTs in order to decrease the size of a TFT so that the effective area of each pixel can be increased as taught in Ikeda (col. 12 lines 1-10)."

35 U.S.C. § 103(a) - Appellants' "admitted prior art" in view of Ikeda et al. in further view of Yamazaki

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Appellants' "admitted prior art" in view of Ikeda and further in view of U.S. Patent Application Publication No. US 2002/0163035 A1 of Yamazaki.

The Office Action acknowledges that "Applicants' admitted prior art fails to teach a signal process circuit formed on the active matrix board for connecting the gate lines and data lines to the gate driving circuit and the signal driving circuit."

The Office Action asserts, however, that "Yamazaki teaches a signal processing circuits (figure 8: 702 and 703) formed on the active matrix board substrate (figure 8:100) and connected to the pixel section 701 through gate wiring 704 and source wiring 158 (Paragraph 135).

The Office Action concludes that "it would have been obvious . . . to have been motivated to have a signal process circuit formed on the active matrix board for connecting the gate lines and data lines to the gate driving circuit and the signal driving circuit as taught in Yamazaki in order to improve the operation

performance and the reliability of a semiconductor device by properly using the TFT structures on the same substrate as taught in Yamazaki (Paragraph 19)."

ARGUMENT

35 U.S.C. § 103(a) - Appellants' "admitted prior art" in view of Ikeda

The rejection of claims 1, 4, and 7 under § 103(a) is in error because the combined disclosures of Appellants' "admitted prior art" and Ikeda would not have rendered obvious the detector defined by any of claims 1, 4, and 7.

First, the disclosures of Appellants' "admitted prior art" and Ikeda, taken as a whole, do not suggest Appellants' claimed detector.

Secondly, the combined disclosures of Appellants' "admitted prior art" and Ikeda do not teach or suggest all of Appellants' claim limitations.

Thirdly, the grounds of rejection constitute an improper reconstruction of Appellants' claimed invention.

Claims 1, 4, and 7

As indicated above, the Office Action asserts (Office Action page 4) with regard to claim 1 that "it would have been obvious . . . to have been motivated to have used poly-silicon as the material for TFTs in order to decrease the size of a TFT so that the effective area of each pixel can be increased as taught in Ikeda (col. 12 lines 1-10)."

The above-quoted portion of the grounds of rejection is in error. Specifically, the rejection is in error because there is no suggestion or motivation in either Appellants' "admitted prior

art" or Ikeda that would have led one to select the references and combine them in a way that would produce the invention defined by any of claims 1, 4, and 7.

To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.

Furthermore, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.

Appellants' claimed invention includes in pertinent part "a converting layer, formed on said pixel electrodes, to generate a pair of electron-holes by absorbing radiation, said converting layer being formed of a vapor-deposited polycrystalline film of CdTe or CdZnTe."

Notwithstanding the assertions of the Examiner, Appellants' claimed radiation detector would not have been obvious because of paragraphs 3, 8 and 10, Figs. 2 and 3 of the "admitted prior art."

Paragraph 3 only discloses "a converting layer 1 of a light conductive layer formed almost all over the surface of the active matrix board 10 . . . ," and fails to disclose wherein the light conductive layer is "a vapor-deposited polycrystalline film of CdTe or CdZnTe," as recited in claims 1 and 7.

Similarly, paragraph 8, only discloses a converting layer 1 to be used that has a light conductivity with respect to not only radiation, such as x-ray, but also the visible light and infrared light. No disclosure of a vapor-deposited polycrystalline film of CdTe or CdZnTe is present.

Furthermore, Figs. 2 and 3 describe the structure of the converter layer in general terms and likewise fails to disclose "a vapor-deposited polycrystalline film of CdTe or CdZnTe," as recited in claims 1 and 7.

Only in paragraph 10, the "admitted prior art" discloses a vapor-deposited polycrystalline film of CdTe or CdZnTe, and then only to say that "there is a difficulty in directly forming a polycrystalline film of a vapor-deposited polycrystalline film of CdTe and CdZnTe on the active matrix board 10 of a-Si:H."

At the time the invention was made, an incompatibility between the heat resistance of TFT and the film forming temperature of CdTe and CdZnTe was known to those knowledgeable in the art. Accordingly, it is not known to directly form a polycrystalline film of CdTe and CdZnTe on pixel electrodes, as recited in claims 1 and 7.

Ikeda is directed to an X-ray image detector system, which includes pixels 801 comprising switching elements 701 using a thin film transistor (TFT) having an active layer of an amorphous silicon, and Se films for X-ray-to-charge converting part deposited on the pixels. Therefore, the detector system of Ikeda uses an amorphous silicon as the TFT, and Se films are deposited thereon. Therefore, the basic structure of claims 1 and 7 are entirely different from the Ex-ray image detector system

In Ikeda, it is held at column 12, lines 1-10 that

> "While Si forming the TFT has been amorphous silicon in the above-described preferred embodiment, the TFT may be formed of a polysilicon. If the TFT is formed of a polysilicon, the size of the TFT can be decreased, so that the effective area of each pixel can be increased. In addition, since peripheral circuits can be prepared on the same glass substrate, it is possible to decrease the production costs including the costs for the peripheral circuits. Furthermore, the structure of the

TFT may be either an upper gate type or a lower gate type."

In this explanation, instead of amorphous silicon, polysilicon can be used, but the purpose of using polysilicon is to reduce the size of the TFT. In the present invention, since the heat resistance of the active matrix board using polysilicon is high to withstand the formation of CdTe and CdZnTe, polysilicon is used. In Ikeda, polysilicon is used only for reducing the size of TFT. Further, even if polysilicon is used in Ikeda, the Se films for the X-ray-to-charge converting part are still deposited on the TFT. Therefore, the detector system in Ikeda is different from the present invention, as a whole.

In the Examiner's rejection, only a part of the invention disclosed in Ikeda was picked up, and the purpose of using the material, i.e. polysilicon, is ignored.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art references. But, even if the references were combined as asserted in the Office Action, they would not result in Appellants' claimed invention. A combination of the applied references would result in a separately formed a vapor-deposited polycrystalline film of CdTe or CdZnTe attached to the pixel electrodes, and not a layer directly formed on the pixel electrodes of the polysilicon TFT, the latter being the subject of Appellants' claimed invention.

Finally, it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.

As indicated above, there is no suggestion in Ikeda of Appellants' claimed "converting layer, formed on said pixel

electrodes, to generate a pair of electron-holes by absorbing radiation, said converting layer being formed of a vapor-deposited polycrystalline film of CdTe or CdZnTe."

Therefore, the only possible manner in which the Examiner could have arrived at his proposed modification is through an improper reconstruction. The examiner's modification is the result of impermissible hindsight derived from first having read Appellants' specification, and is an improper reconstruction of the claimed invention using Appellant's own disclosure as a roadmap for selectively combining the applied prior art references.

Appellants submit, therefore, that the grounds of rejection presented in the Office Action fail to establish a *prima facie* case of obviousness with respect to each of claims 1, 4, and 7.

35 U.S.C. § 103(a) - Appellants' "admitted prior art" in view of Ikeda and further in view of Yamazaki

For all of the reasons identified above with respect to the rejection of claims 1, 4, and 7, the rejection of claim 5 is also in error.

Claim 5

Dependent claim 5, which depends from claim 4 and indirectly from claim 1, is allowable along with claims 1 and 4, and on its own merits.

Claim 5 adds the further limitation of "a gate driving circuit to be connected to the gate lines, a signal reading circuit to be connected to the data lines, and a signal process circuit formed on the active matrix board for connecting the

gate lines and data lines to the gate driving circuit and the signal reading circuit."

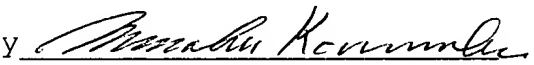
Regardless of what Yamazaki may disclose with regard to signal processing circuits, the disclosure of Yamazaki does not rectify the above-described deficiencies of the "admitted prior art" and Ikeda. The claimed invention would not have been obvious because even if the references were combined as asserted in the Office Action, they would not result in Appellants' claimed invention.

Appellants submit, therefore, that the grounds of rejection presented in the Office Action fail to establish a *prima facie* case of obviousness with respect to claim 5.

Appellants respectfully submit that the rejections of claims 1, 4, 5, and 7 under § 103(a) are in error, and request that each of the final rejections be reversed.

Respectfully submitted,

KANESAKA BERNER AND PARTNERS

By 

Manabu Kanesaka
Reg. No. 31,467
Agent for Appellants

1700 Diagonal Road, Suite 310
Alexandria, VA 22314
(703) 519-9785

CLAIMS APPENDIX

1. A radiation detector comprising:

an active matrix board including gate lines and data lines arranged in a two-dimensional lattice shape, a plurality of high-speed switching elements provided at respective lattice points and connected to the gate lines and the data lines, each switching element being formed of a polycrystalline silicon thin film transistor and having a source electrode, pixel electrodes connected to the source electrodes of the high-speed switching elements, and charge storage capacitances, each being disposed between the pixel electrode and a ground electrode; and

a converting layer, formed on the pixel electrodes, to generate a pair of electron-holes by absorbing radiation, said converting layer being formed of a vapor-deposited polycrystalline film of CdTe or CdZnTe.

4. A radiation detector according to claim 1, wherein said active matrix board further includes a base plate having high heat resistance and insulating properties, an insulating film disposed on the base plate and sandwiched by the gate lines and data lines, an insulating protective layer disposed on the insulating film above the switching element, and a common electrode disposed on the converting layer.

5. A radiation detector according to claim 4, further comprising a gate driving circuit to be connected to the gate lines, a signal reading circuit to be connected to the data lines, and a signal process circuit formed on the active matrix board for connecting the gate lines and data lines to the gate driving circuit and the signal reading circuit.

7. A radiation detector comprising:

an active matrix board including gate lines and data lines arranged in a two-dimensional lattice shape, a plurality of high-speed switching elements provided at respective lattice points and connected to the gate lines and the data lines, each switching element being formed of a polycrystalline silicon thin film transistor with a heat resistant temperature of more than 300°C and having a source electrode, pixel electrodes connected to the source electrodes of the high-speed switching elements, and charge storage capacitances, each being disposed between the pixel electrode and a ground electrode; and

a converting layer, formed on the pixel electrodes, to generate a pair of electron-holes by absorbing radiation, said converting layer being a vapor-deposited polycrystalline film of CdTe or CdZnTe having a film-forming temperature higher than 300°C.

EVIDENCE APPENDIX

No copies of evidence are appended hereto.

RELATED PROCEEDINGS APPENDIX

No copies of decisions are appended hereto.